WHAT IS CLAIMED IS:

1. A diagnostic system associated with a microprocessor, comprising:

a state machine adapted to change its internal state in response to a trigger event generated by the microprocessor, and adapted to halt the microprocessor in response to a predetermined combination of the trigger event and a preceding internal state of the state machine prior to the trigger event;

a backup register adapted to save the preceding state when the state machine changes state in response to the trigger event; and

state restoration logic adapted to use the backup register to restore the state machine to its preceding state if the trigger event is invalid.

2. The diagnostic system as recited in claim 1, wherein trigger events comprise specified memory addresses.

3. The diagnostic system as recited in claim 2, wherein trigger events further comprise specified data values.

4. The diagnostic system as recited in claim 1, wherein the microprocessor is equipped with an instruction pipeline.

5. The diagnostic system as recited in claim 1, wherein the microprocessor further comprises an exception handler that returns execution to a branch instruction, upon returning from an exception associated with the instruction immediately following the branch instruction.

6. The diagnostic system as recited in claim 5, wherein the trigger event is invalid whenever the branch instruction is re-executed upon returning from the exception handler.

7. The diagnostic system as recited in claim 1, further comprising an enhanced joint test action group (EJTAG) compliant interface.

8. The diagnostic system as recited in claim 1, further comprising a trace function, adapted to output the current location of the microprocessor program counter while the microprocessor executes program instructions.

9. A method for saving and restoring states of a diagnostic module, comprising:

providing a diagnostic module adapted to change its state in response to trigger events generated by a microprocessor and to halt the microprocessor in response to a specified combination of trigger events and previous states;

saving the previous state of the diagnostic module in a backup register; and

if the trigger event is not valid, using the backup register to restore the diagnostic module to its previous state.

10. The method as recited in claim 9, wherein generating a trigger event comprises issuing a specified memory address.

11. The method as recited in claim 10, wherein generating a trigger event further comprises accessing a specified data value.

12. The method as recited in claim 9, wherein the microprocessor is equipped with an instruction pipeline.

13. The method as recited in claim 9, wherein the microprocessor further comprises an exception handler that returns execution to a branch instruction, upon returning from an exception associated with the instruction immediately following the branch instruction.

14. The method as recited in claim 13, further comprising generating an invalid trigger event by re-executing the branch instruction upon returning from the exception handler.

15. A microprocessor, with an associated diagnostic module, said module comprising:

a state machine, adapted to change its internal state in response to trigger events generated by the microprocessor, and adapted to halt the microprocessor in response to a trigger event and preceding internal state prior to the trigger event;

a backup register, adapted to save the preceding state of the state machine when it changes state in response to the trigger event; and

state restoration logic, adapted to use the backup register to restore the state machine to its preceding state, if the trigger event is invalid.

16. The diagnostic system as recited in claim 15, wherein trigger events comprise specified memory addresses.

17. The diagnostic system as recited in claim 15, wherein trigger events further comprise specified data values.

18. The diagnostic system as recited in claim 15, wherein the microprocessor further comprises an exception handler that returns execution to a branch instruction, upon returning from an exception associated with the instruction immediately following the branch instruction.

19. The diagnostic system as recited in claim 15, wherein an invalid trigger event comprises a branch instruction that is re-executed upon returning from the exception handler.